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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/484,549	01/18/2000	Korbin Van Dyke	01000.9901080	9816

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EXAMINER	
ALI, SYED J	

ART UNIT	PAPER NUMBER
2127	

DATE MAILED: 07/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/484,549	VAN DYKE ET AL.	
	Examiner	Art Unit	
	Syed J Ali	2127	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-12 and 14-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-12 and 14-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 January 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed May 3, 2004. Claims 2-12 and 14-17 are presented for examination.

2. The text of those sections of Title 35, U.S. code not included in this office action can be found in a prior office action.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. **Claims 14 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Leondires et al. (USPN 5,841,763) (hereinafter Leondires).**

5. As per claim 17, Leondires teaches the invention as claimed, including an apparatus comprising:

a plurality of processors coupled to a bus (col. 9 lines 26-49);

an input/output interface coupled to the bus (col. 9 lines 26-49);

a plurality of input/output devices coupled to the input/output interface col. 9 lines 26-49), the plurality of processors processing program code configured to perform a plurality of tasks (col. 9 lines 50-64), the program code comprising:

program code configured to cause a first portion of the plurality of processors to interact with a first input/output device of the plurality of input/output devices (col. 17 line 51 - col. 18 line 8);

program code configured to cause a second portion of the plurality of processors to interact with a second input/output device of the plurality of input/output devices (col. 17 line 51 - col. 18 line 8);

program code configured to cause a second portion of the plurality of processors to emulate a specific microprocessor instruction set (col. 9 lines 50-64; col. 18 lines 9-18; col. 18 line 63 - col. 19 line 7);

wherein the first portion of the plurality of processors provide functionality as found in a first application-specific subsystem and wherein the first input/output device is the first application-specific subsystem (col. 9 lines 50-64; col. 18 lines 9-18; col. 18 line 63 - col. 19 line 7); and

wherein the second portion of the plurality of processors provide functionality as found in a second application-specific subsystem and wherein the second input/output device is the second application-specific subsystem (col. 9 lines 50-64; col. 18 lines 9-18; col. 18 line 63 - col. 19 line 7).

6. As per claim 14, Leondires teaches the invention as claimed, including the apparatus of claim 17 further comprising:

kernel program code configured to dynamically allocate the processing of the program code among the plurality of processors (col. 4 lines 60-67).

Claim Rejections - 35 USC § 103

7. **Claims 2-3, 5-12, and 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leondires in view of Carmon et al. (USPN 5,724,587) (hereinafter Carmon).**

8. As per claim 15, Leondires teaches the invention as claimed, including a method for providing multimedia functionality in a homogeneous multiprocessor environment comprising the steps of:

identifying available processing resources in the homogeneous multiprocessor environment (col. 3 line 35 - col. 4 line 5);

allocating the available processing resources among the tasks based on the capabilities of each of the available processing resources and the processing requirements of each of the tasks (col. 3 line 35 - col. 4 line 5; col. 17 lines 35-50; col. 18 lines 19-36); and

providing to the available processing resources functional programs and initial data corresponding to the tasks (col. 9 lines 50-64; col. 18 lines 9-18; col. 18 line 63 - col. 19 line 7); and

performing the tasks using the available processing resources to produce resulting data (col. 17 line 35 - col. 18 line 8).

9. Carmon teaches the invention as claimed, including the following limitations not shown by Leondires:

queuing tasks (col. 3 lines 50-61).

10. It would have been obvious to one of ordinary skill in the art to combine Leondires and Carmon since the queuing of incoming signals into packets such that the processors may simply look on a queue for a next task greatly improves the processing efficiency of the system. A simple distribution of tasks could result in a bottleneck condition where the processors cannot process the signals as fast as they are received. This may lead to any number of failure conditions. The queuing of incoming tasks allows the host to continue to distribute the tasks, resulting in greater throughput.

11. As per claim 2, Leondires teaches the invention as claimed, including the method of claim 15 wherein a plurality of processors of the homogeneous multiprocessor environment are capable of executing a first instruction of a first instruction set and a second instruction of a second instruction set (col. 9 lines 50-64; col. 18 lines 9-18; col. 18 line 63 - col. 19 line 7).

12. As per claim 3, Leondires teaches the invention as claimed, including the method of claim 2 wherein the first instruction and the second instruction share an identical bit pattern but perform different operations (col. 16 lines 37-61).

13. As per claim 5, Leondires teaches the invention as claimed, including the method of claim 3 further comprising the step of:

converting a functional program of the functional programs expressed using the first instruction set to an equivalent functional program expressed using the second

instruction set (col. 9 lines 50-64; col. 16 lines 37-61; col. 18 lines 9-18; col. 18 line 63 - col. 19 line 7).

14. As per claim 6, Leondires teaches the invention as claimed, including the method of claim 3 wherein the tasks comprise:

x86 processing (col. 16 lines 18-35);

graphic image processing (col. 16 lines 18-35);

video processing (col. 16 lines 18-35);

audio processing (col. 16 lines 18-35); and

communication processing (col. 16 lines 18-35).

15. As per claim 7, Leondires teaches the invention as claimed, including the method of claim 3 further comprising the step of:

receiving the initial data from a first input/output device (col. 16 lines 37-61; col. 19 lines 9-18).

16. As per claim 8, Leondires teaches the invention as claimed, including the method of claim 3 further comprising the step of:

passing the resulting data to a first input/output device (col. 17 line 35 - col. 18 line 8).

17. As per claim 9, Leondires teaches the invention as claimed, including the method of claim 8 wherein the step of passing the resulting data to the first input/output device further comprises the step of:

passing the resulting data through an intermediary device, wherein the intermediary device is coupled to the first input/output device and to a second input/output device (col. 17 line 35 - col. 18 line 8).

18. As per claim 10, Leondires teaches the invention as claimed, including the method of claim 9 wherein the step of passing the resulting data through an intermediary device, wherein the intermediary device is coupled to the first input/output device and to a second input/output device further comprises the step of:

automatically adapting to a reallocation of the available processing resources among the tasks (col. 4 lines 60-67).

19. As per claim 11, Leondires teaches the invention as claimed, including the method of claim 8 wherein the step of passing the resulting data to a first input/output device further comprises the step of:

passing the resulting data to a mixed-signal device (col. 17 line 35 - col. 18 line 8).

20. As per claim 12, Leondires teaches the invention as claimed, including the method of claim 3 wherein the step of allocating the available processing resources among the tasks is dynamically adjusted (col. 4 lines 60-67).

21. As per claim 16, Leondires teaches the invention as claimed, including a method for providing multimedia functionality in a homogeneous multiprocessor environment comprising the steps of:

keeping track, remotely from the resources, of the capabilities of all available processing resources (col. 3 line 35 - col. 4 line 5);

identifying available processing resources in the homogeneous multiprocessor environment based solely on the capabilities kept track of remotely (col. 3 line 35 - col. 4 line 5);

allocating the available processing resources among the tasks based on the capabilities of each of the available processing resources and the processing requirements of each of the tasks (col. 3 line 35 - col. 4 line 5; col. 17 lines 35-50; col. 18 lines 19-36);

providing to the available processing resources functional programs and initial data corresponding to the tasks (col. 9 lines 50-64; col. 18 lines 9-18; col. 18 line 63 - col. 19 line 7); and

performing the tasks using the available processing resources to produce resulting data (col. 17 line 35 - col. 18 line 8).

22. Carmon teaches the invention as claimed, including the following limitations not shown by Leondires:

queuing tasks (col. 3 lines 50-61).

23. It would have been obvious to one of ordinary skill in the art to combine Leondires and Carmon for reasons discussed above in reference to paragraph 10.

24. **Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Leondires in view of Carmon in view of Guyer et al. (USPN 4,597,041) (hereinafter Guyer).**

25. As per claim 4, Guyer teaches the invention as claimed, including the following limitations not shown by Leondires or Carmon:

the method of claim 3 wherein a first processor of the plurality of processors executes an input/output kernel program, the input/output kernel program including a first portion expressed using the first instruction set and a second portion expressed using the second instruction set (col. 17 lines 25-37).

26. It would have been obvious to one of ordinary skill in the art to combine Leondires and Carmon with Guyer since the availability of multiple instruction sets increases the capabilities of a system. Specifically, executing a kernel such that it is compatible with multiple instruction sets allows the system to interact with many different types of devices, and eliminates certain hardware needs. For instance, a system with devices implemented in different instruction sets would normally require a specific processor for each instruction set. By allowing a single processor to execute instructions of different instruction sets, the need for an additional processor is eliminated, increasing the efficiency of that system.

Response to Arguments

27. Applicant's arguments with respect to claims 2-12 and 14-17 have been considered but are moot in view of the new grounds of rejection.

Conclusion

27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Syed J Ali whose telephone number is (703) 305-8106. The examiner can normally be reached on Mon-Fri 8-5:30, 2nd Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai T An can be reached on (703) 305-9678. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Syed Ali
July 6, 2004

LEWIS A. BULLOCK, JR.
PRIMARY EXAMINER